REMARKS/ARGUMENTS

This Amendment is submitted in response to the Final Office Action dated August 10, 2005, and within the period for response extending to November 10, 2005. The status of the claims is summarized as follows:

Claim 14 is currently amended;

Claims 12 and 24 are cancelled; and

Claims 1-11, 13-23, and 25-29 remain pending after entry of this Amendment.

Allowable Subject Matter

The Applicants acknowledge the Office's indication that claims 14 and 15 would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112, 2nd paragraph, and to include all of the limitations of the base claim and any intervening claims.

The Applicants acknowledge the Office's indication that claims 8, 13, 18, 25, 26, and 28 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Specification

The Office has not indicated an objection to the specification in the Office Action Summary. However, in the "Response to Arguments" section of the Detailed Action, the Office continues to object to the specification based on the assertion that "pull down logic 221" as described in paragraph [0028] is misleading. The Office asserts that circuit 221 is a latch rather than pull down logic.

The Applicants respectfully disagree with the Office's assertion that circuit 221 is a latch. The functionality of the pull down logic 221 is described in the following excerpt from paragraph [0028] of the specification:

> "The inputs of NMOS devices M1 and M2 are connected to sense nodes SN and SN_l, respectively. However, the gates of NMOS devices M1 and M2 are connected to sense nodes SN_l and SN, respectively. Thus, as sense node SN_l begins to attain a higher state relative to sense node SN, NMOS device M1 will begin to transmit causing the state of SN to become lower. Conversely, as sense node SN begins to attain a higher state relative to sense node SN_l, NMOS device M2 will being to transmit causing the state of SN_l to become lower. Therefore, NMOS devices M1 and M2 serve to pull down sense nodes SN and SN_l, respectively, as the complementary sense node begins to attain a higher state."

In accordance with the description of the pull down logic 221 in paragraph [0028], it should be appreciated that the term "pull down logic" provides a clear and precise description of the cross-coupled NMOS devices M1 and M2 and their configuration in the sense stage 205 of the sense amplifier 201. The Office is respectfully reminded that the Applicants are entitled to be their own lexicographer. The Applicants believe that changing the name "pull down logic 221" to "latch", as suggested by the Office, would be misleading and incorrect.

In view of the foregoing, the Applicants do not believe it is appropriate to change the term "pull down logic 221" to "latch" as suggested by the Office. Therefore, the Office is again respectfully requested to withdraw the objection to the specification associated with use of the term "pull down logic 221."

Rejections under 35 U.S.C. 112

Claims 14 and 15 have been rejected under 35 U.S.C. 112, 2nd paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These rejections are traversed.

With respect to claim 14, the Office has asserted that the recitation "a pair of charging devices each being configured to supply a steady voltage to a separate one of the pair of input nodes upon receipt of a recovery activation signal" is indefinite because it is not clear. The Office has also asserted that claim 15 is indefinite because of the indefiniteness of claim 14.

The Office is requested to note that claim 14 has been amended to recite "a pair of charging devices each being configured to supply a steady voltage to a separate one of the pair of input nodes." The pair of charging devices recited in claim 14 corresponds to the PMOS devices M6 and M7 as shown in Figure 2B. The Applicants submit that amended claim 14 satisfies the requirements of 35 U.S.C. 112, 2nd paragraph. Additionally, based on the clarifying amendments to claim 14, the Applicants submit that claim 15 satisfies the requirements of 35 U.S.C. 112, 2nd paragraph.

In view of the foregoing, the Applicants submit that each of claims 14 and 15 particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. Therefore, the Office is requested to withdraw the rejections under 35 U.S.C. 112, 2nd paragraph.

Rejections under 35 U.S.C. 102

Claims 1-4, 6, 7, 9-11, 16, 19-23, and 29 were rejected under 35 U.S.C. 102(b) as being anticipated by Su et al. ("Su" hereafter) (U.S. Patent No. 6,275,435). These rejections are traversed.

The Office has asserted that the sense amplifier as depicted in Figure 1 of Su teaches each and every feature of claim 1. For example, the Office has asserted that PMOS devices 18_1, 18_2 in Figure 1 of Su represent a pair of booster circuits that are each configured to assist in a low-to-high state transition of a separate one of the pair of sense nodes during a sensing operation. The Office has referenced nodes $N11B_2$ and $N11_2$ in Figure 1 of Su as representing the pair of sense nodes. Thus, with respect to Figure 1 of Su, the Office asserts that the PMOS devices 18_1, 18_2 assist in a low-to-high state transition of a separate one of nodes $N11B_2$ and $N11_2$, during a sensing operation.

Claim 1 recites the following:

> "the sense stage includes a pair of booster circuits, each of the pair of booster circuits being configured to assist in a low-to-high state transition of a separate one of the pair of sense nodes during a sensing operation."

The PMOS devices 18_1 and 18_2 of Su are part of a precharge circuit that is not enabled during a sensing operation. More specifically, Su (column 1, lines 43-48) teaches that passgates 18_1 and 18_2 for a precharge circuit that is controlled by a signal PRECHB1, which is asserted to provide conductive paths between sense amplifier nodes ($N11B_2$ and $N11_2$) and a power supply voltage Vdd. Su (column 1, lines 52-55) further teaches that when signals EQUALIZE and PRECHB1 are both asserted, datalines DLB and DL (including nodes $N11B_2$ and $N11_2$) are precharged to a level substantially equal to the level of supply voltage Vdd.

It should be appreciated that a precharge operation and a sensing operation cannot be simultaneously performed with respect to sense amplifier nodes $N11B_2$ and $N11_2$. For example, during the precharge operation a conduction path is formed between sense nodes $N11B_2$ and $N11_2$ by turning on PMOS devices 18_1 and 18_2. With a conduction path formed between sense nodes $N11B_2$ and $N11_2$ during the precharge operation, it would be

impossible to sense a voltage present on either of sense nodes $N11B_2$ and $N11_2$ because the sense nodes $N11B_2$ and $N11_2$ would essentially become a common node. Furthermore, turning on PMOS devices 18_1 and 18_2 during the precharge operation will always drive both sense nodes $N11B_2$ and $N11_2$ to Vdd, thus removing any possibility of performing a sensing operation in conjunction with the precharge operation. Therefore, it is not reasonable to conclude that PMOS devices 18_1 and 18_2 can function as booster circuits to assist in a low-to-high state transition of the sense nodes $N11B_2$ and $N11_2$ during a sensing operation.

For at least the reasons discussed above, Su fails to teach each and every feature of claim 1, as required to support an anticipation rejection under 35 U.S.C. 102. Therefore, the Applicants submit that claim 1 is patentable over the cited art of record. Also, the Applicants submit that each of claims 2-4 and 6-7 is patentable with respect to Su for at least the same reasons provided for claim 1, from which it depends. Therefore, the Applicants respectfully request the Office to withdraw the rejections of claims 1-4 and 6-7.

With respect to claim 9, the Office has asserted that PMOS devices 18_1, 18_2 in Figure 1 of Su represent a pair of booster circuits configured to assist in a low-to-high state transition of a respective one of the pair of sense nodes during a sensing operation. Therefore, the arguments presented above with respect to claim 1 are equally applicable to claim 9. Consequently, Su fails to teach each and every feature of claim 9, as required to support an anticipation rejection under 35 U.S.C. 102.

For at least the reasons provided above, the Applicants submit that claim 9 is patentable over the cited art of record. Also, the Applicants submit that each of claims 10-11, 16, and 19 is patentable with respect to Su for at least the same reasons provided for

claim 9, from which it depends. Therefore, the Applicants respectfully request the Office to withdraw the rejections of claims 9-11, 16, and 19.

With respect to claim 20, the Office has asserted that PMOS devices 18_1, 18_2 in Figure 1 of Su represent a pair of booster circuits configured to assist in a low-to-high state transition of the sense node to which the booster device is connected during a sensing operation. Therefore, the arguments presented above with respect to claims 1 and 9 are equally applicable to claim 20. Consequently, Su fails to teach each and every feature of claim 20, as required to support an anticipation rejection under 35 U.S.C. 102.

For at least the reasons provided above, the Applicants submit that claim 20 is patentable over the cited art of record. Also, the Applicants submit that each of claims 21-23 and 29 is patentable with respect to Su for at least the same reasons provided for claim 20, from which it depends. Therefore, the Applicants respectfully request the Office to withdraw the rejections of claims 20-23 and 29.

Rejections under 35 U.S.C. 103

Claims 5, 17, and 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over McClure. These rejections are traversed.

Because each of dependent claims 5, 17, and 27 ultimately depends from independent claims 1, 9, and 20, respectively, and incorporates all features of its respective independent claim, the Applicants submit that each of dependent claims 5, 17, and 27 is patentable for at least the reasons provided above for its respective independent claim. Therefore, the Applicants respectfully request the Office to withdraw the rejections of dependent claims 5, 17, and 27.

In view of the foregoing, the Applicants submit that claims 1-11, 13-23, and 25-29 are in condition for allowance. Therefore, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 774-6914. If any additional fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP383). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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